REMARKS:

Applicants are amending claims 1, 4, 7, 11-12, 15, 18 and 19. Thus, claims 1-20 currently are pending and are subject to examination in the above-captioned patent application. No new matter is added by the foregoing amendments, and these amendments are fully supported by the specification. Applicants respectfully request that the Examiner reconsider the above-captioned patent application in view of the foregoing amendments and the following remarks.

In the Office Action mailed August 10, 2005, the Examiner rejected claims 1, 2, 5, 6, 15, 16 and 20 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Chi (U.S. Patent No. 6,501,109) in view of Suzuki (U.S. Patent No. 6,816,198). The Examiner also rejected claims 3 and 17 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Chi in view of Suzuki and further in view of Yamauchi et al. (U.S. Patent No. 5,075,888, hereinafter "Yamauchi"). Moreover, the Examiner rejected claim 18 under 35 U.S.C. § 103(a)m as allegedly being rendered obvious by Chi in view of Suzuki and further in view of Lee et al. (U.S. Patent Publication No. 2002/0214379, hereinafter "Lee"). Further, the Examiner rejected claims 4 and 19 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Chi in view of Suzuki and further in view of Chi et al. (U.S. Patent No. 6,060,742, hereinafter "Chi '742"). The Examiner also rejected claims 7-10 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Chi in view of Yamauchi. Moreover, the Examiner rejected claims 11, 13, and 14 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Chi in view of Lee. Further, the Examiner rejected claim 12 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Chi in view of Lee and further in view of Chi '742.

To the extent that these rejections remain applicable in view of the foregoing amendments, Applicants respectfully traverse these rejections, as follows.

Applicants have amended each of independent, apparatus claims 1, 7, and 11 to describe, in part, a solid-state image pickup device comprising "a first gate structure including a charge storage region and a control gate, said first gate structure being formed on a surface of said semiconductor substrate adjacent to a portion of said first region, and said **charge storage region being electrically isolated from said first region**." Applicants also have amended independent, method claim 15 to include corresponding method limitations.

In contrast to Applicants' claimed invention as set forth in independent claims 1, 7, 11, and 15, Chi merely discloses an image pickup device that exploits gate induced drain leakage (GIDL) current to create an output that is exponential relative to a stored charge. In particular, Chi describes an image pickup device having a p-type semiconductor substrate 70, an n-well 40 formed in the substrate 70, a first p+-type region formed in the n-well and constituting a photodiode 38 with the n-well 40, and a second p+-type region formed in the n-well 40 and constituting an output diode 42 with the n-well 40. Chi also describes a floating gate 44 formed over the output diode 42, **the floating gate 44 being shorted to the p+-floating node of the photodiode 38**, and a control gate 46 coupled to the output diode 42 and the photodiode 38. Chi further describes a metal plug connected to the output diode 42, which is connected to a metal line.

In Chi, charges are accumulated on the surface of the second p+-type region (i.e., the output diode 42) by band-to-band tunneling. The charges create the gate-

induced-drain-leakage (GIDL) current, which is provided to a sense amplifier by the output diode 42 during a read operation. To enhance the GIDL current, Chi discloses using an n-type doped floating gate 44, a p-type doped control gate 46, eliminating silicide on the output diode 42 (which prevents band-to-band tunneling and thus, the GIDL current), and omitting the lightly doped drain (LDD) implant structures on the p+-type regions 38 and 42 and the spacer structure at the floating-gate edge.

However, in Chi, because the floating gate 44 is shorted to the p+-floating node of the photodiode 38, Chi does not disclose or suggest at least the feature that the charge storage region is electrically isolated from the first region that includes the associated photodiode, as set forth in Applicants' independent claims 1, 7, 11, and 15, as amended.

Applicants also have amended independent claim 7 to describe, in part, a solid-state image pickup device comprising "an optical window formed on said first region and made of transparent material."

In contrast to Applicants' claimed invention as set forth in independent claim 7, Figure 9 of Yamauchi depicts a photodiode that consists of a p-Si substrate 8, a n-diffusion region 4, a floating gate 6, and a MOS transistor that consists of n-diffusion region 4, p-Si substrate 8, a n-diffusion region 1, and a gate G1. However, Yamauchi's structure has a control gate CG that is disposed above the photodiode. Yamauchi discloses at col. 8, lines 50-52, "when the photodiode PD is irradiated by a light beam, electrons (minor carrier) generate in the p-Si substrate 8 and move to the n-diffusion layer 4". This indicates that incident light is irradiated to the p-Si substrate 8 side, not to the n-diffusion layer 4 side. If incident light is irradiated to n-diffusion layer 4 from

above, the control gate CG will **shield the incident light to the photodiode**. In contrast, Applicants' claimed invention, as set forth in independent claim 7, as amended, includes an optical window made of **transparent material** formed on the photodiode. Therefore, Applicants respectfully request that the Examiner withdraw the obviousness rejections of claims 1, 7, 11, and 15 at least for these reasons.

Claims 2-6, 8-10, 12-14, and 16-20 depend from allowable, independent claims 1, 7, 11, and 15, respectively. Therefore, Applicants respectfully request that the Examiner withdraw the obviousness rejections of claims 2-6, 8-10, 12-14, and 16-20 at least for this reason.

CONCLUSION:

Applicants respectfully submit that the above-captioned patent application is in condition for allowance, and such action is earnestly solicited. If the Examiner believes that an in-person or telephonic interview with Applicants' representatives would expedite the prosecution of the above-captioned patent application, the Examiner is invited to contact the undersigned attorney of records. Applicants are enclosing a check in the amount of $120.00 covering the requisite large entity fee for a one-month extension of time to respond to the outstanding Office Action in the above-captioned patent application. Nevertheless, in the event of any variance between the fees determined by Applicants and those determined by the U.S. Patent and Trademark Office, please charge or credit any such variance to the undersigned's Deposit Account No. 01-2300, referencing Attorney Docket No. 107317-00061.

Respectfully submitted,

Wilburn L. Chesser
Attorney for Applicants
Registration No. 41,668

Customer No. 004372
ARENT FOX, PLLC
1050 Connecticut Ave., N.W., Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 715-8434
Facsimile No. (202) 638-4810

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Enclosure: Petition for Extension of Time (one month)